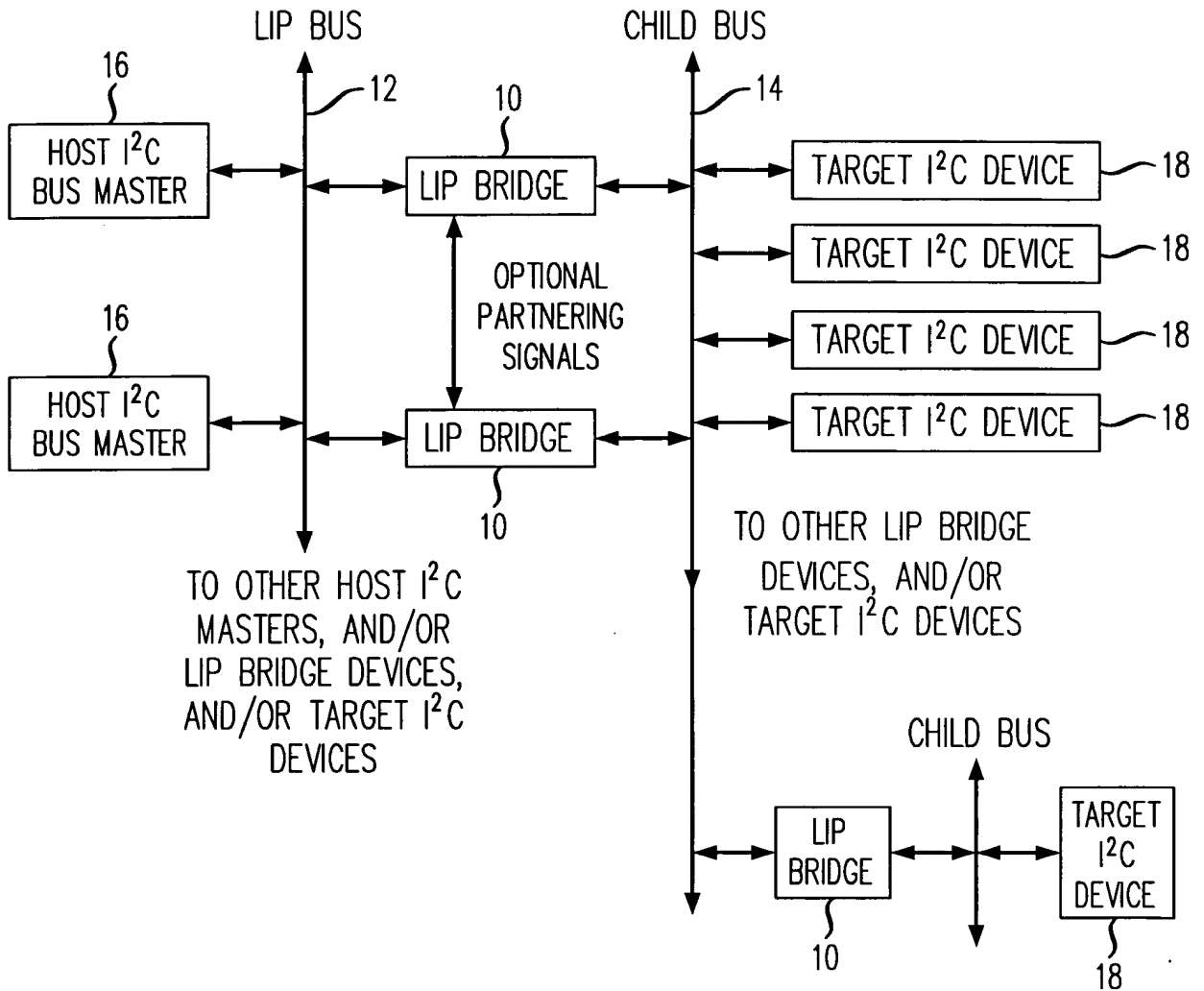




Drawing Approved
OEC 12/3/03

FIG. 1
TYPICAL LIP BRIDGE USAGE




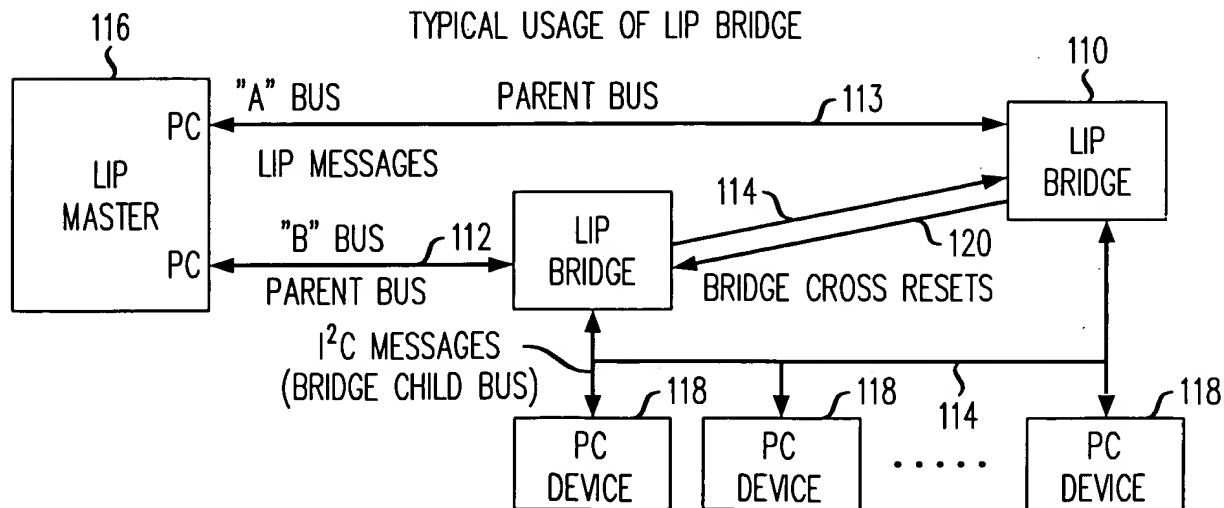


FIG. 2

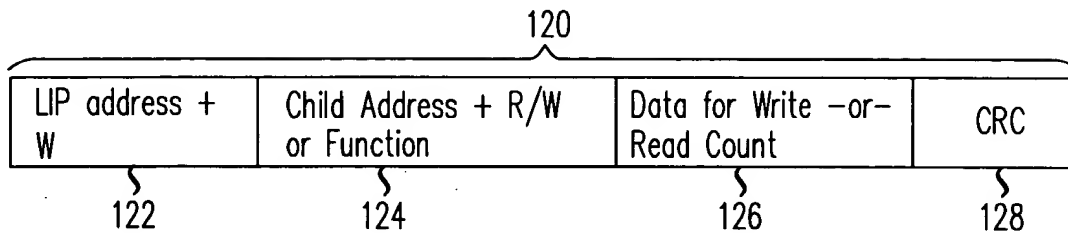
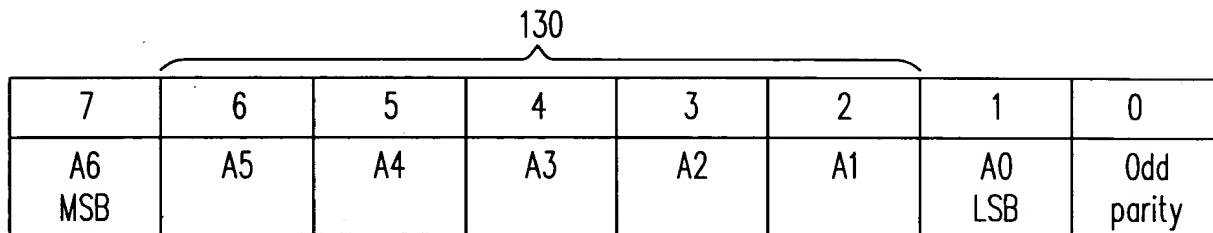
The diagram illustrates the internal architecture of a LIP Bridge. It features two main buses: the LIP BUS (top left) and the CHILD BUS (top right). The LIP BUS connects to a LIP BUS I²C TRANSCEIVER (20), which interfaces with a BRIDGE READ ENGINE (24) and a CRC GENERATOR AND CHECKER (22). The BRIDGE READ ENGINE also connects to INCOMING LIP PACKET INCOMING FIFO (30). The CRC GENERATOR AND CHECKER outputs to OUTGOING LIP PACKET FIFO 0 (28) and OUTGOING LIP PACKET FIFO 1 (29). These FIFOs feed into the LIP PACKET PARSER&DISPATCH (32). The CHILD BUS connects to a CHILD BUS I²C TRANSCEIVER (50), which interfaces with an ERROR LOGGER (40) and an ERROR LOG (41). The ERROR LOGGER also feeds into the LIP PACKET PARSER&DISPATCH. A COMMAND COLLISION DETECTION unit (38) receives inputs from the LIP PACKET PARSER&DISPATCH and the ERROR LOGGER. The LIP PACKET PARSER&DISPATCH outputs to a SPECIAL FUNCTION COMMAND ENGINE (36) and a CHILD BUS COMMAND ENGINE (36). The SPECIAL FUNCTION COMMAND ENGINE outputs to OUTGOING LIP PACKET FIFO 0 and OUTGOING LIP PACKET FIFO 1. The CHILD BUS COMMAND ENGINE outputs to the CHILD BUS I²C TRANSCEIVER. External components include a GLOBAL RESET (42), GLOBAL WATCHDOG (44), LIP SUPPLY VOLTAGE MONITOR (46), and EVENT WATCHDOG TIMER (56), all connected to the system via a common bus (48).

TYPICAL USAGE OF LIP BRIDGE



"Replacement Sheet"

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**FIG. 4****FIG. 5**

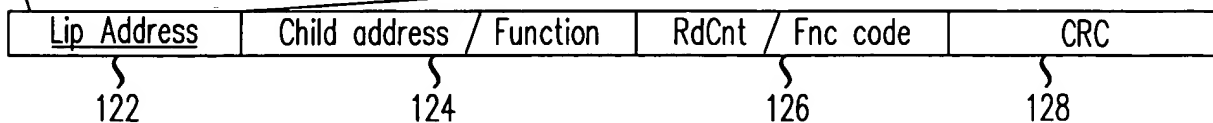
Hardware Address Strapping

FIG. 6

The LIP Address / Function encoding within the four byte LIP packet is as follows:

Lip address

7	6	5	4	3	2	1	0
A6 MSB	A5	A4	A3	A2	A1	A0 LSB	R/!W





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FIG. 7

The Child Address / Function Encoding is as follows:

Child Address / Function

7	6	5	4	3	2	1	0
MSB	...					LSB	R/W

LIP Address	Child address / Function	Wr data / RdCnt / Fnc code	CRC
122	124	126	128

FIG. 8

Read Count Field

7 MSB	6	5	4	3	2	1	0 LSB
Rsvd-0	Srcl'd	RdCnt					

LIP Address	Child Bus Address	Read Count field	CRC
122	124	126	128

FIG. 9

Read Data Tag

7 MSB	6	5	4	3	2	1	0 LSB
No Data	Srcl'd	RdCnt					

LIP Address + R	Read Data Tag	RdCnt data bytes	CRC
138	136	134	142
	132	130	

FIG. 10

Status Byte Register Organization

RAZ	RAZ	RAZ	ME	LBWE	LBRE	CBWE	CBRE
MSB							LSB

150



FIG. 11

TABLE 8

Key to Symbols	
Symbol	Meaning
S	I ² C bus start condition
P	I ² C bus stop condition
A	Acknowledge
A	No-Acknowledge
LA	LIP address
CA	Child bus address
W	R/W bit within address field is set for WRITE
R	R/W bit within address field is set for READ
CRC	CRC byte
Data	Data byte
Count	Read count
Fn(x)	Special function command "x" - where x is the function's hex code
	Gray shade indicates data sent from Host Bus to LIP bridge
	White indicates data sent from LIP bridge to Master
.....	Zero or more instances of the preceding transaction.

Host bus master to LIP One Byte Child Bus Write

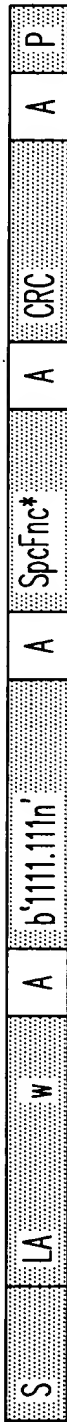


} 160

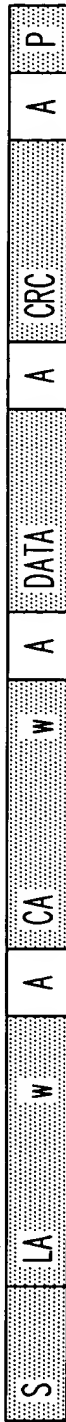


FIG. 12

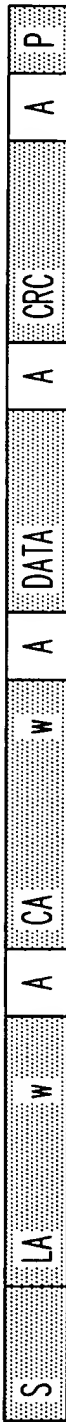
Host bus master to LP Multi-Byte Write



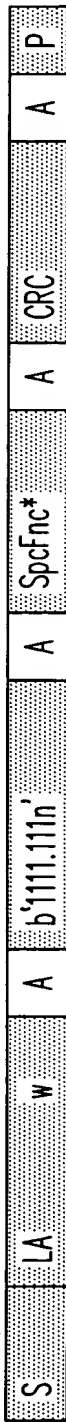
* Child I²C start



.....

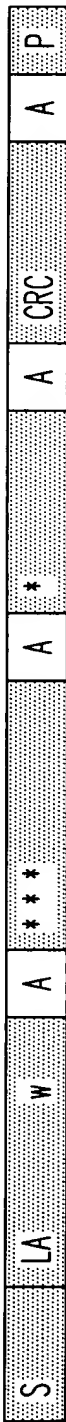


To complete transaction, either:



OR

Child I²C stop



Where: n=0 for host bus master 0 and n=1 for host bus master 1. The "***" CA field contains a different value than that contained in the first data packet (SECOND PACKET ABOVE). This can be either a different child address, or it can be a special function indicator of binary '1111.111n'.

FIG. 13

Special Function Action Returning Nor Requiring Data

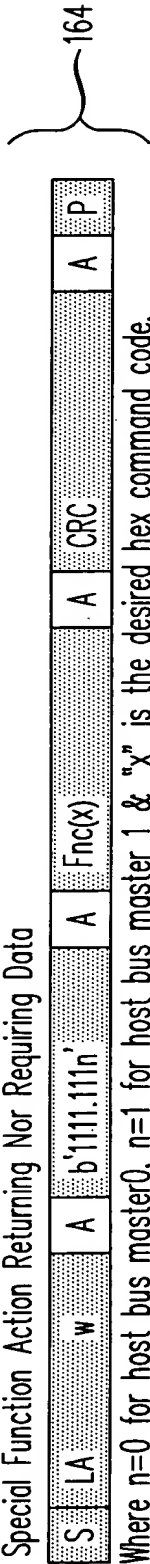


FIG. 14

Special Function Action Returning Data

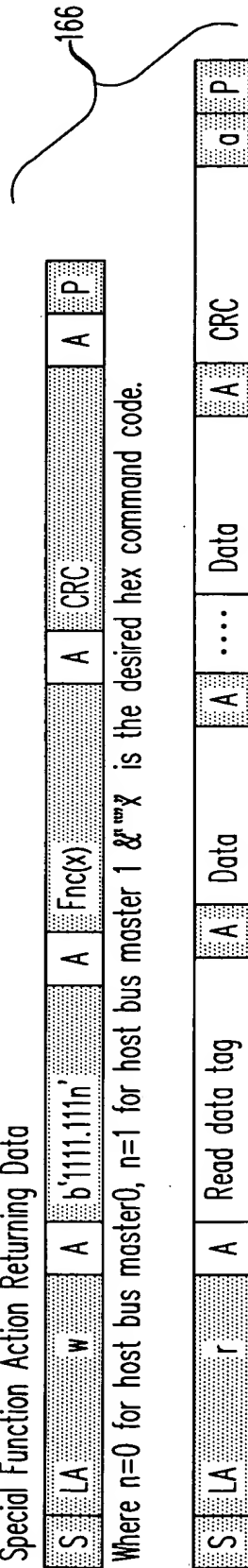


FIG. 15

Special Function Action Requiring Data

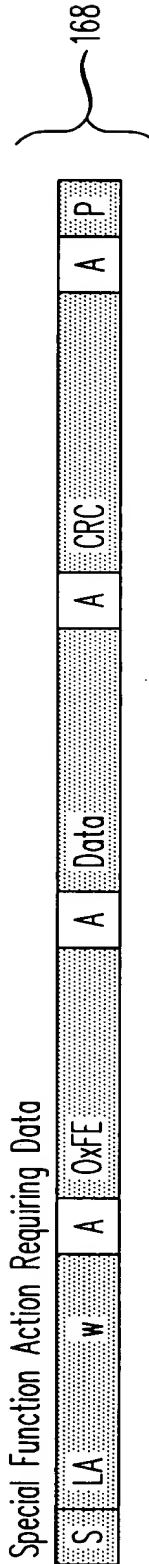
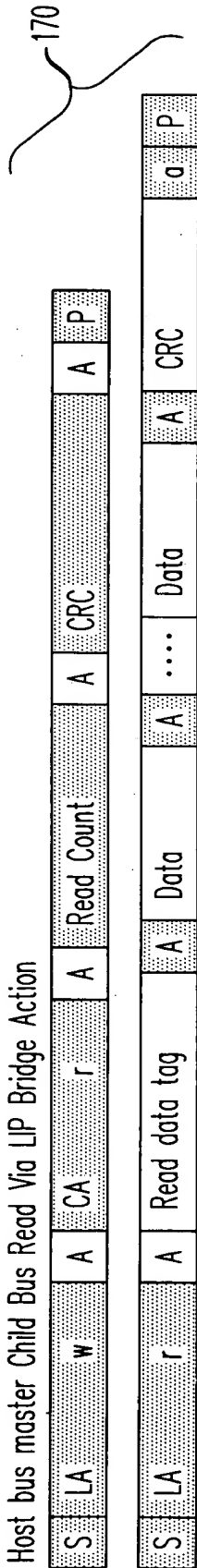


FIG. 16

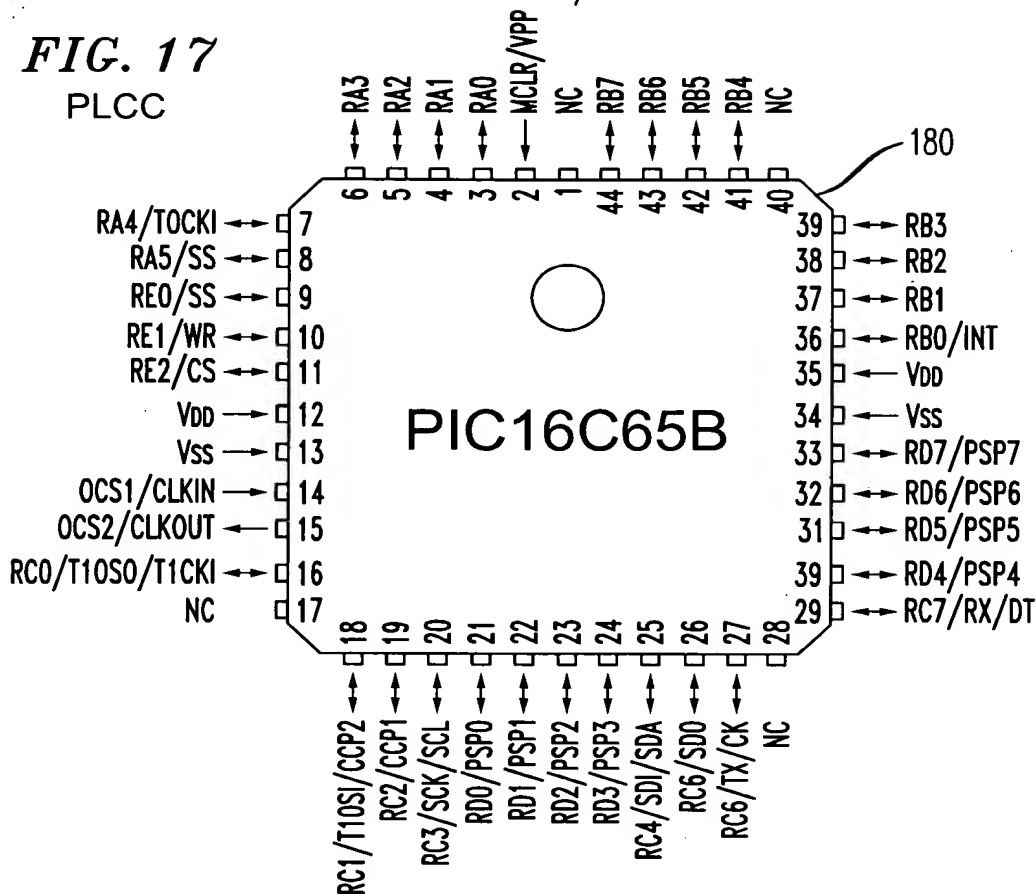
Host bus master Child Bus Read Via LIP Bridge Action



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FIG. 17

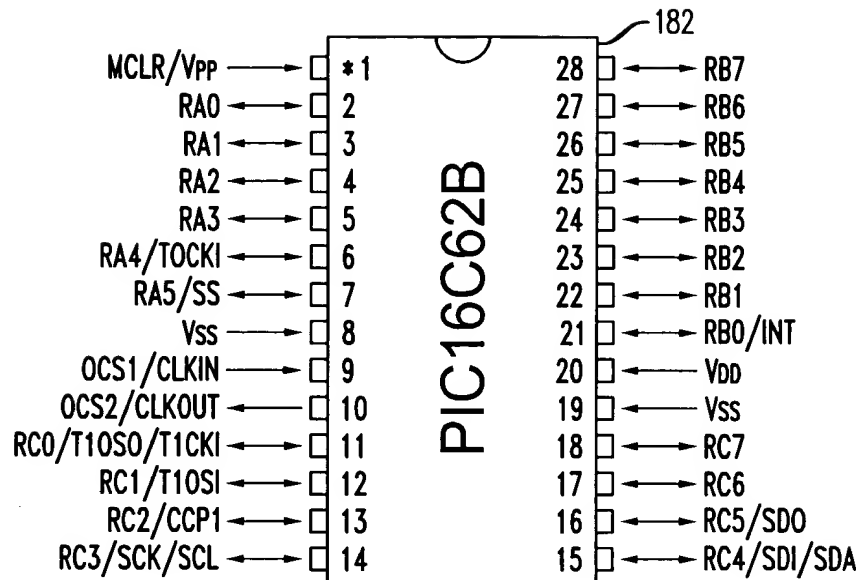
PLCC



PIN #	Label	Function
2	!MCLR	!partner_reset_in - Active low input for reset from partner LIP bridge (Also VPP pin for in circuit programming)
3	RA0	!partner_reset_out - Active low output to reset partner LIP bridge
20	RC3	LIP_clk - LIP bus serial clock in
25	RC4	LIP_data - LIP bus serial data in/out (bidirectional)
27	RC6	child_clk - child bus clock output
29	RC7	child_data - child bus data in/out (bidirectional)
37	RB1	LIP_addr_parity - parity bit for LIP address (strap to make odd parity)
38	RB2	LIP_addr0 - bit 0 to strap LIP I ² C address
39	RB3	LIP_addr1 - bit 1 to strap LIP I ² C address
41	RB4	LIP_addr2 - bit 2 to strap LIP I ² C address
42	RB5	LIP_addr3 - bit 3 to strap LIP I ² C address
4	RA1	LIP_addr4 - bit 4 to strap LIP I ² C address
5	RA2	LIP_addr5 - bit 5 to strap LIP I ² C address
43	RB6	In circuit programming clock
44	RB7	In circuit programming data
6	RA3	child_bus_busy_out - active low open collector output when this LIP bridge owns child bus (needs a 1K pull up to Vdd).
36	RB0	child_bus_busy_in - active low input when partner LIP bridge owns child bus



FIG. 18

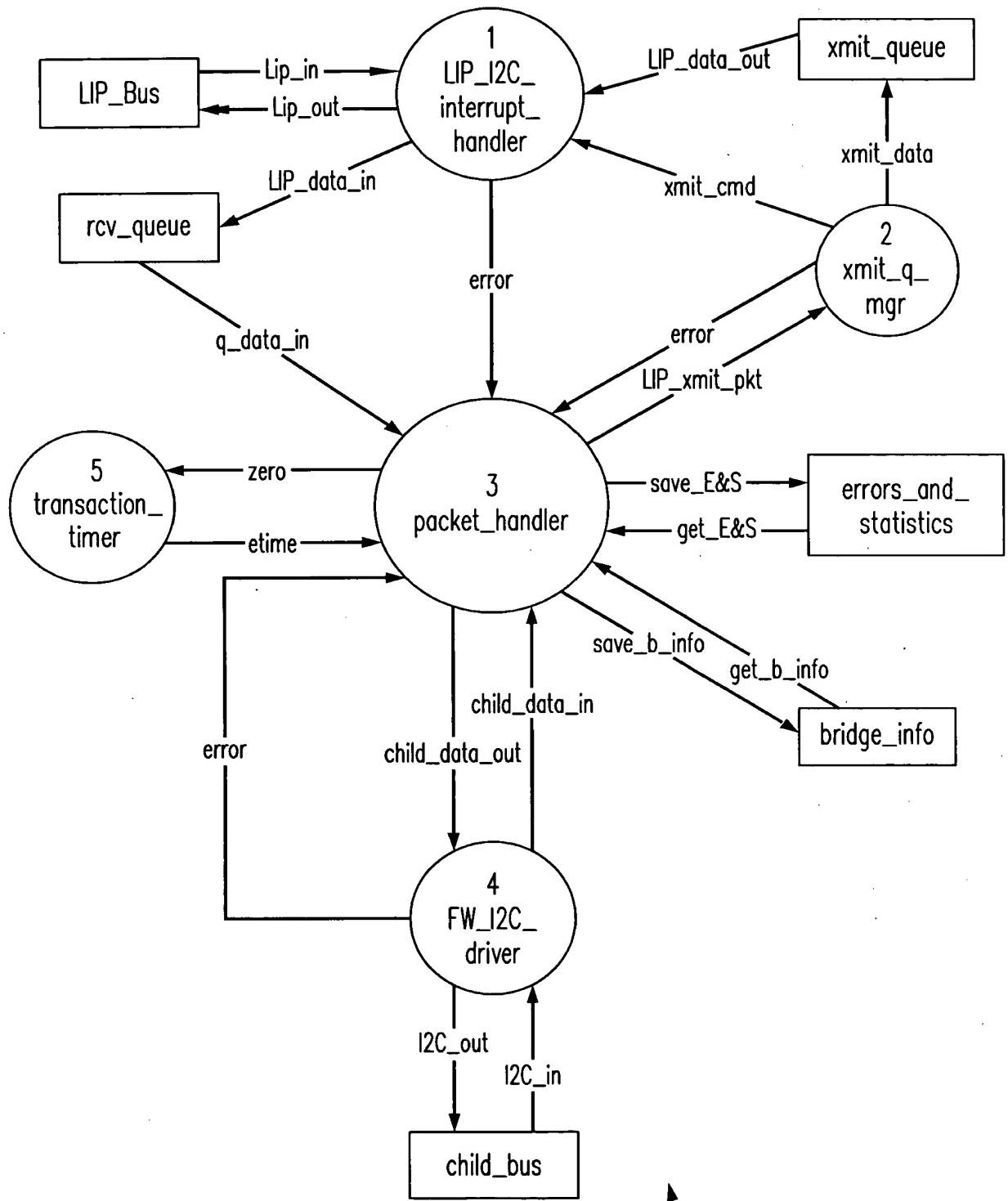


PIN #	Label	Function
1	!MCLR	!partner_reset_in – Active low input for reset from partner LIP bridge (Also VPP pin for in circuit programming)
2	RA0	!partner_reset_out – Active low output to reset partner LIP bridge
14	RC3	LIP_clk – LIP bus serial clock in
15	RC4	LIP_data – LIP bus serial data in/out (bidirectional)
17	RC6	child_clk – child bus clock output
18	RC7	child_data – child bus data in/out (bidirectional)
22	RB1	LIP_addr_parity – parity bit for LIP address (strap to make odd parity)
23	RB2	LIP_addr0 – bit 0 to strap LIP I ² C address
24	RB3	LIP_addr1 – bit 1 to strap LIP I ² C address
25	RB4	LIP_addr2 – bit 2 to strap LIP I ² C address
26	RB5	LIP_addr3 – bit 3 to strap LIP I ² C address
3	RA1	LIP_addr4 – bit 4 to strap LIP I ² C address
4	RA2	LIP_addr5 – bit 5 to strap LIP I ² C address
27	RB6	In circuit programming clock
28	RB7	In circuit programming data
5	RA3	child_bus_busy_out – active low output when this LIP bridge owns child bus (needs a 1K pull up to Vdd).
21	RB0	child_bus_busy_in – active low input when partner LIP bridge owns child bus



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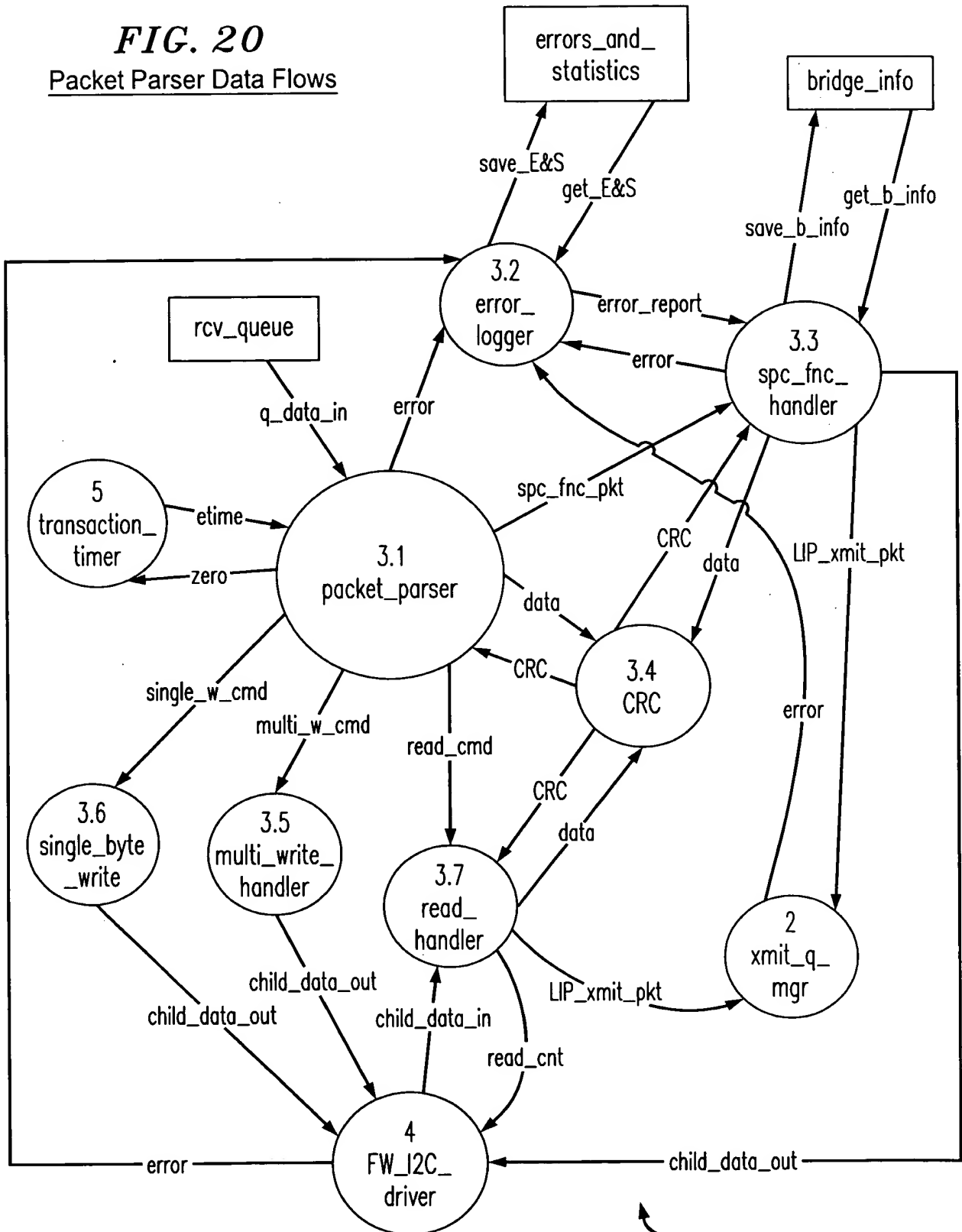
FIG. 19
Level 1 Data Flow Diagram





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FIG. 20
Packet Parser Data Flows





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FIG. 21

Firmware I2C Data Flows

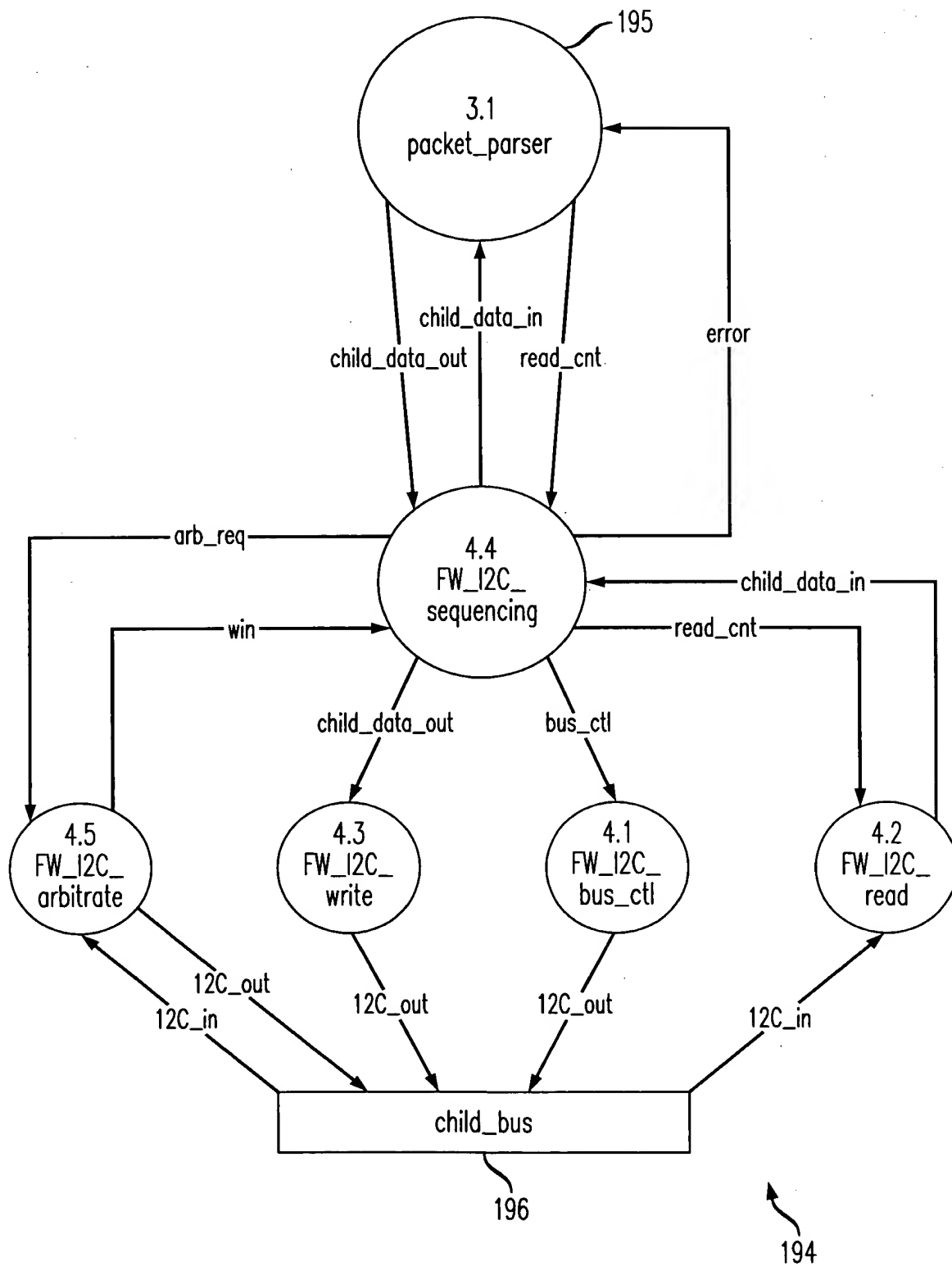




FIG. 22

